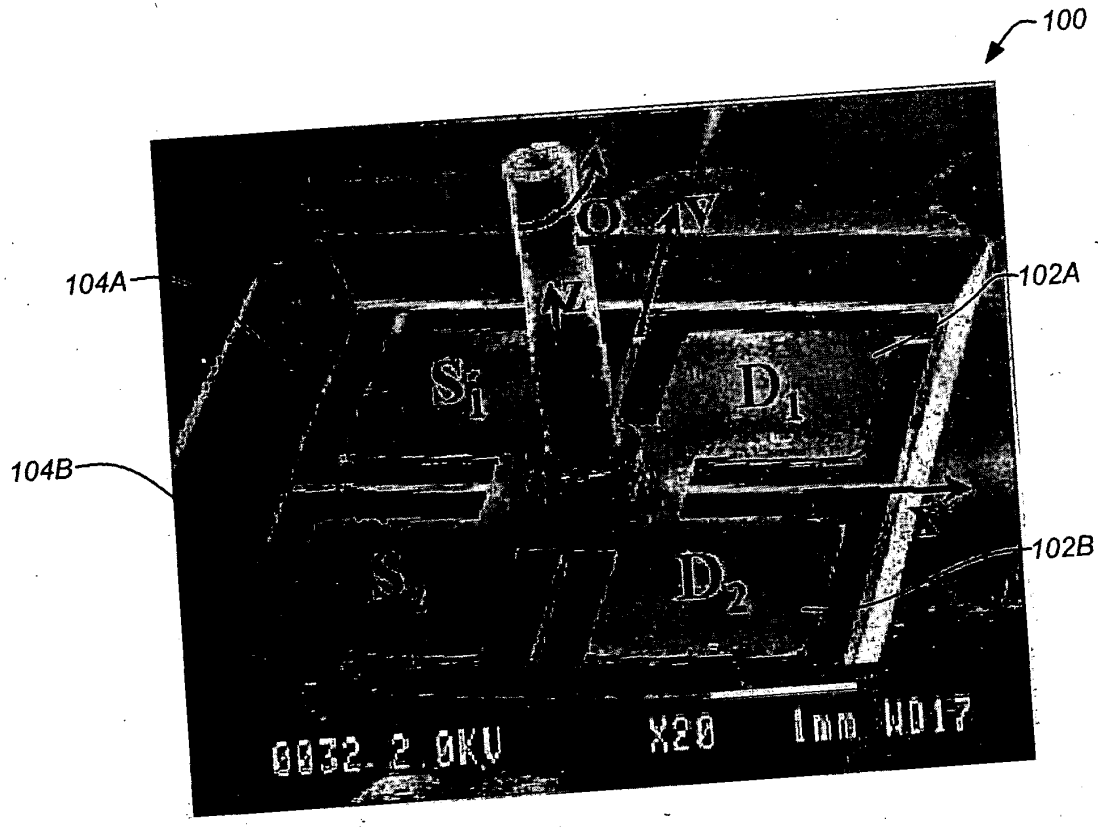

FIG. 1A

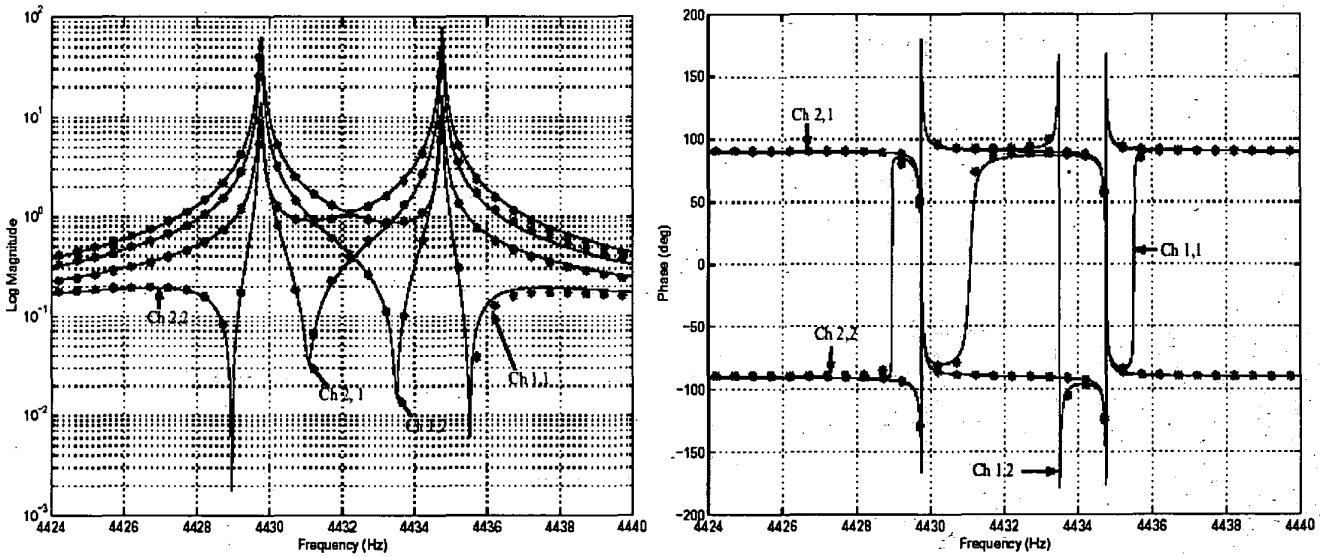
Log Magnitude
Frequency (Hz)
Ch 2,2
Ch 2, 1
Ch 1,1
Ch 1,2
Phase (deg)
Ch 2,1
Ch 2,2
Ch 1,1
Ch 1,2

FIG. 1B

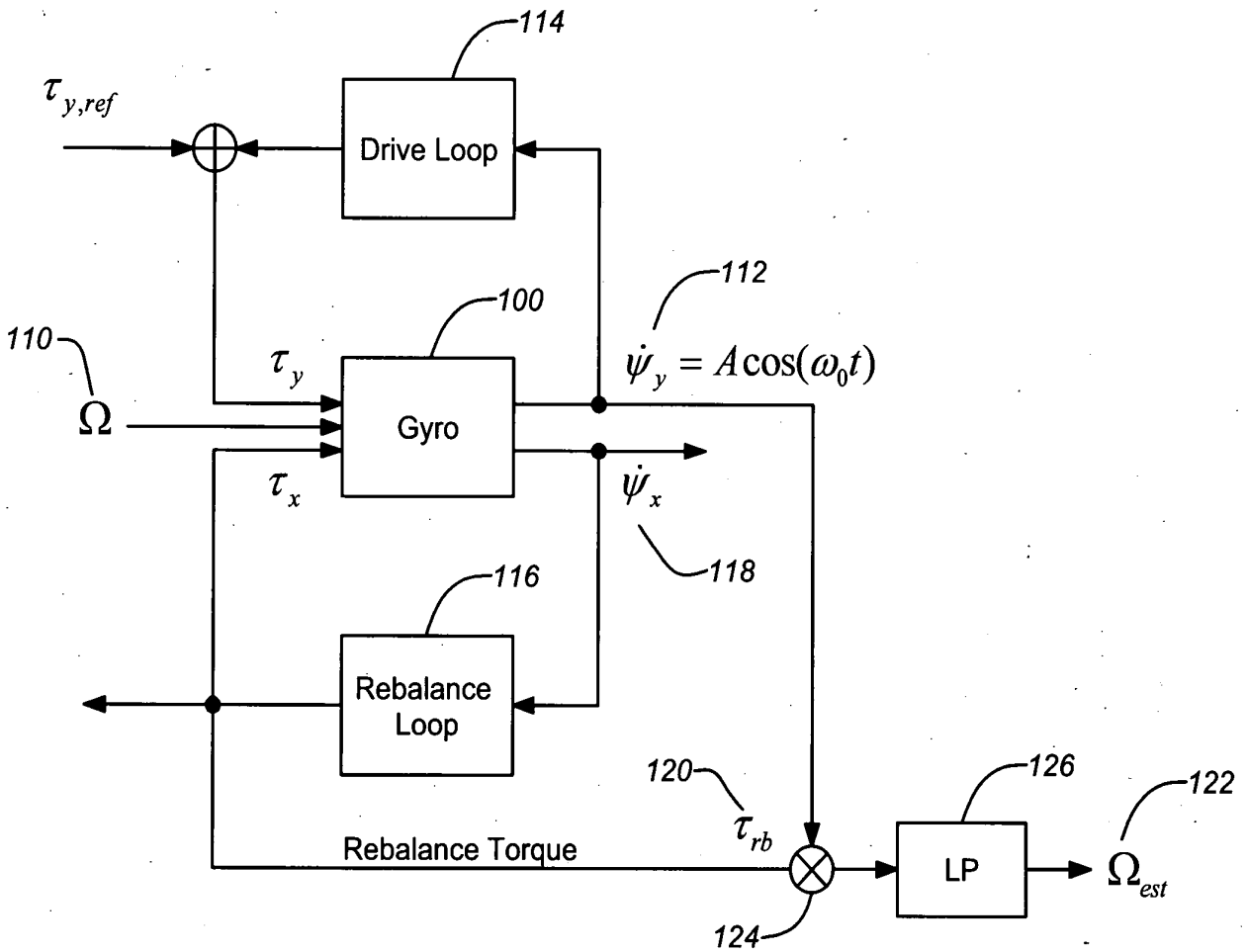
114
$\tau_{y,ref}$
Drive Loop
112
100
110
τ_y
$\dot{\psi}_y = A\cos(\omega_0 t)$
Ω
Gyro
τ_x
$\dot{\psi}_x$
118
116
Rebalance Loop
120
126
122
τ_{rb}
Rebalance Torque
LP
Ω_{est}
124

FIG. 1C

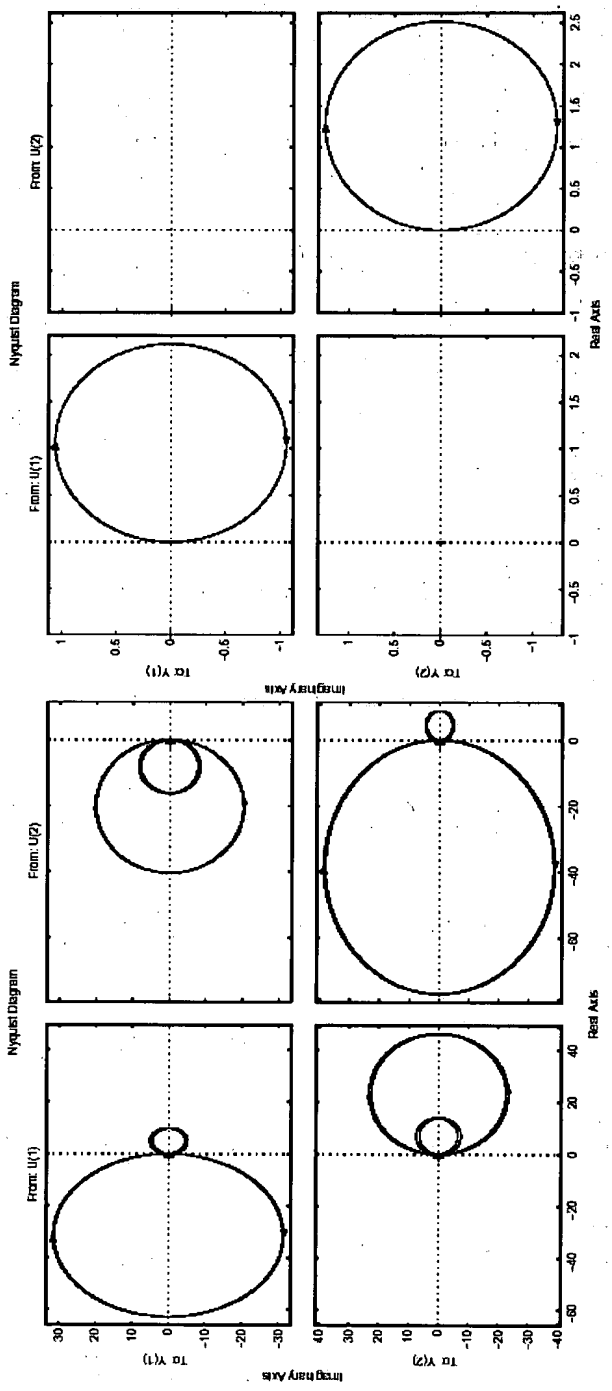
Nyquist Diagram
From: U(1)
From: U(2)
To: Y(1)
To: Y(2)
Imaginary Axis
Real Axis

FIG. 1D

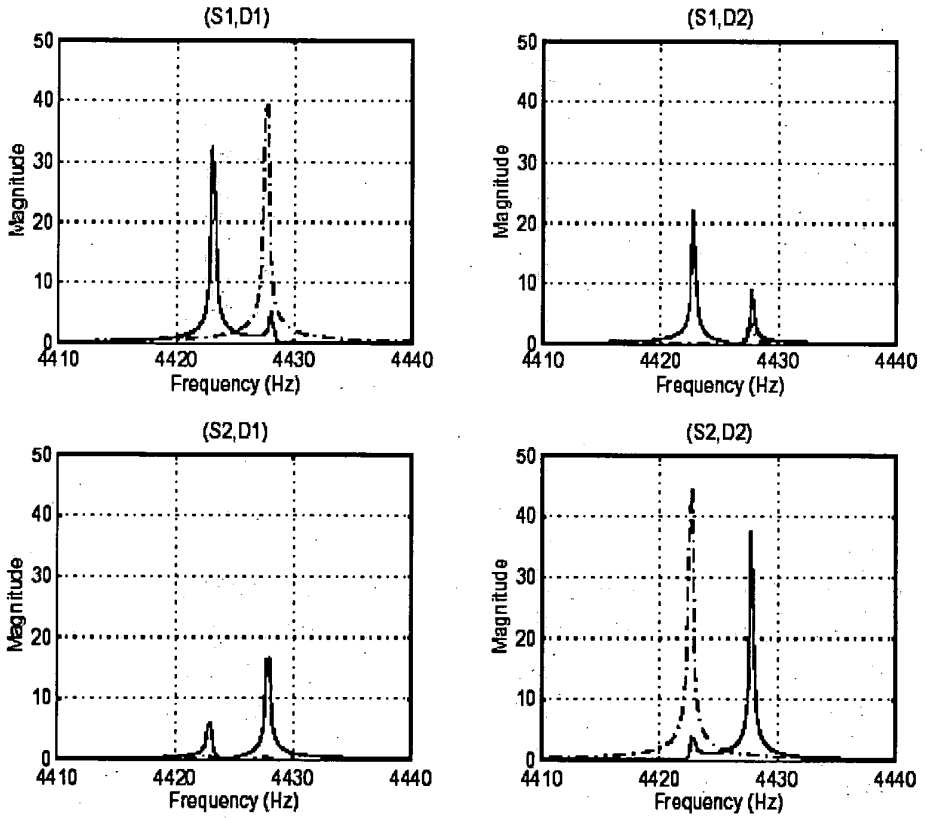
(S1,D1)
(S1,D2)
(S2,D1)
(S2,D2)
Magnitude
Frequency (Hz)
0
10
20
30
40
50
4410
4420
4430
4440

FIG. 1E

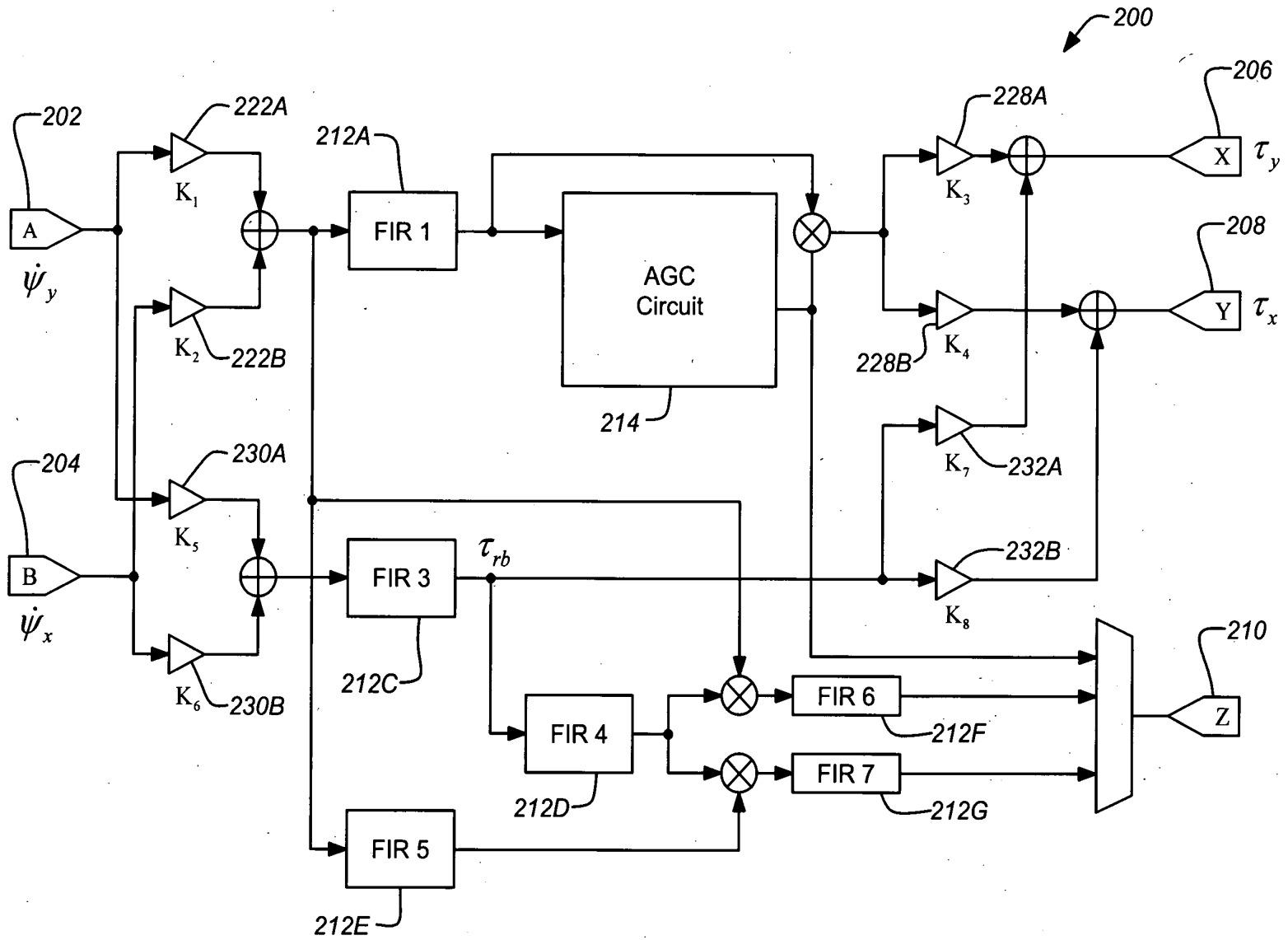
200
202
222A
212A
206
228A
A
$\dot{\psi}_y$
K_1
FIR 1
K_3
X
τ_y
AGC
Circuit
208
K_2
222B
228B
K_4
Y
τ_x
214
K_7
232A
204
230A
K_5
B
$\dot{\psi}_x$
FIR 3
τ_{rb}
232B
K_8
K_6
230B
212C
210
FIR 6
Z
FIR 4
212F
FIR 7
212D
212G
FIR 5
212E

FIG. 2A

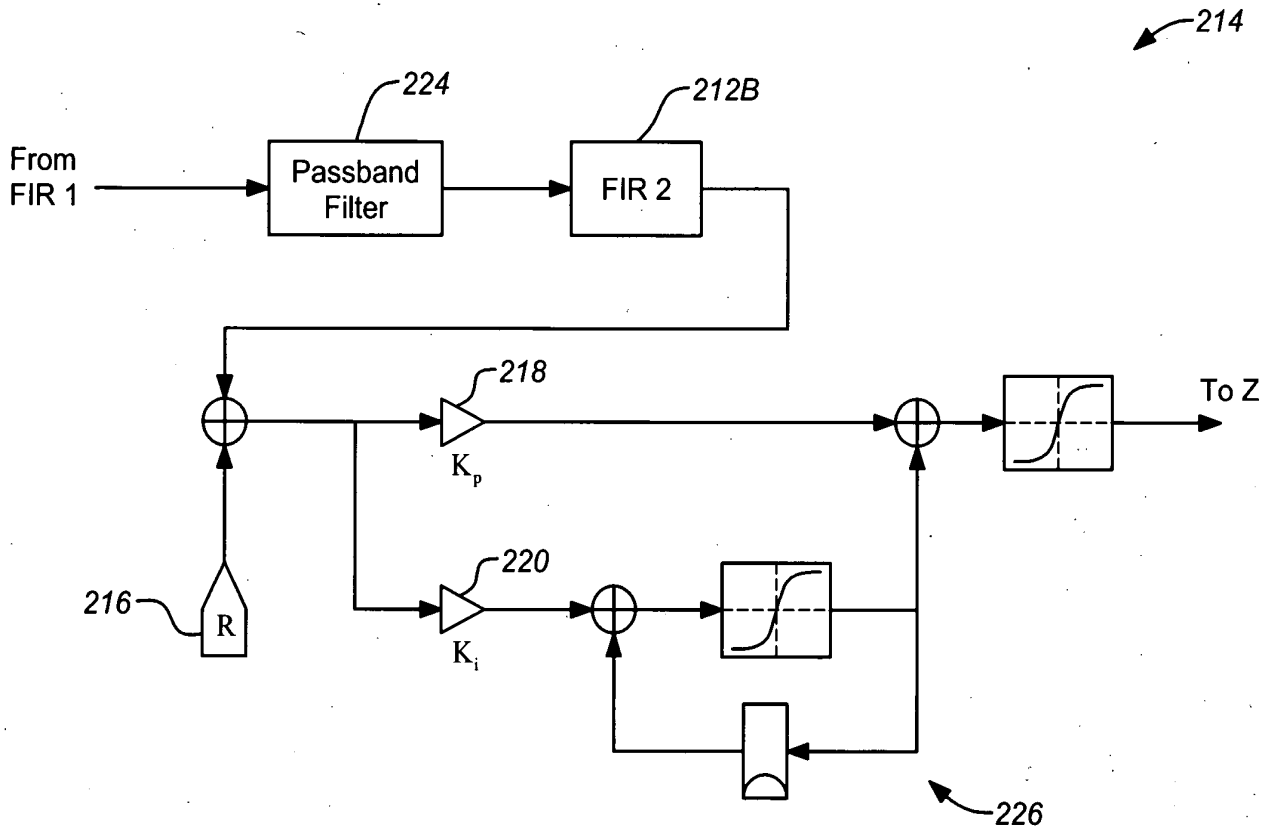
214
224
212B
From
FIR 1
Passband
Filter
FIR 2
218
K_p
To Z
220
216
R
K_i
226

FIG. 2B

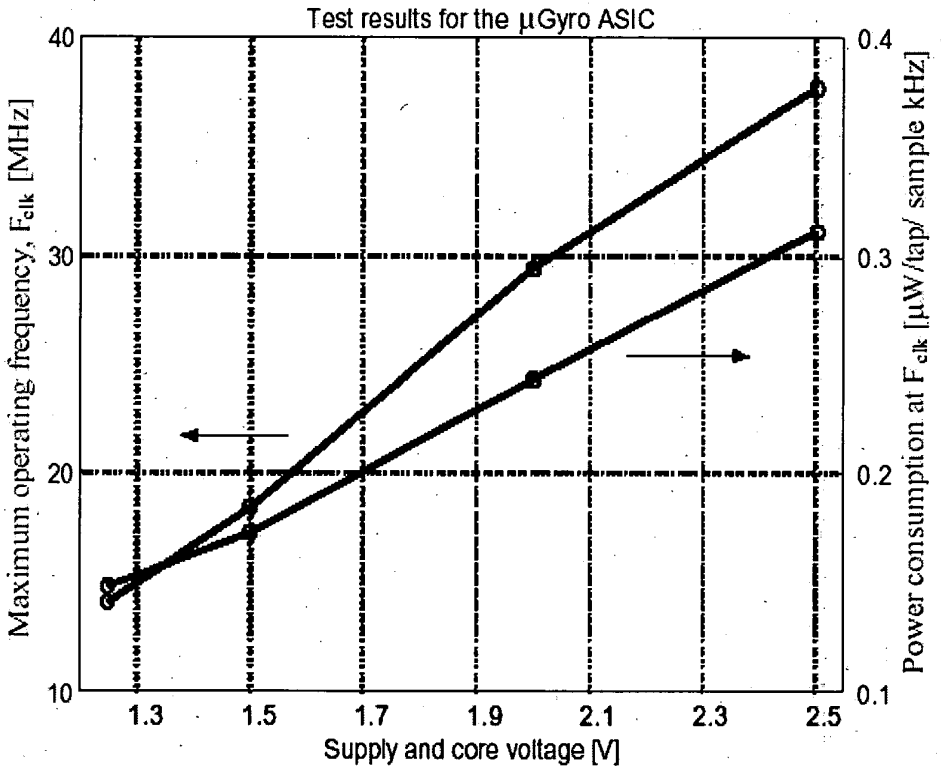
Test results for the µGyro ASIC
Maximum operating frequency, F_{clk} [MHz]
Power consumption at F_{clk} [µW/tap/ sample kHz]
Supply and core voltage [V]
40
30
20
10
0.4
0.3
0.2
0.1
1.3
1.5
1.7
1.9
2.1
2.3
2.5

FIG. 3A

Parameter	Symbol	Conditions	min	typ	max	Units
Power Supply IO	PVDD		1.25		2.5	V
Power Supply CORE	CVDD	CVDD ≤ PVDD	1.25		2.5	V
Power Dissipation IO	P_{IO}	VDD=2.5V		0.13		µW/tap/ kHz
Power Dissipation CORE	P_{CORE}			0.18		
Input High Voltage	V_{IH}		PVDD			V
Input Low Voltage	V_{IL}		0			V
Master Clock Frequency	F_{CLK}	VDD=2.5V	0		37	MHz
Interface Clock Frequency	F_{CLK_INT}		≤ $F_{CLK}/2$			MHz
Supply at F_{CLK}=20MHz	VDD		1.6			V

FIG. 3B

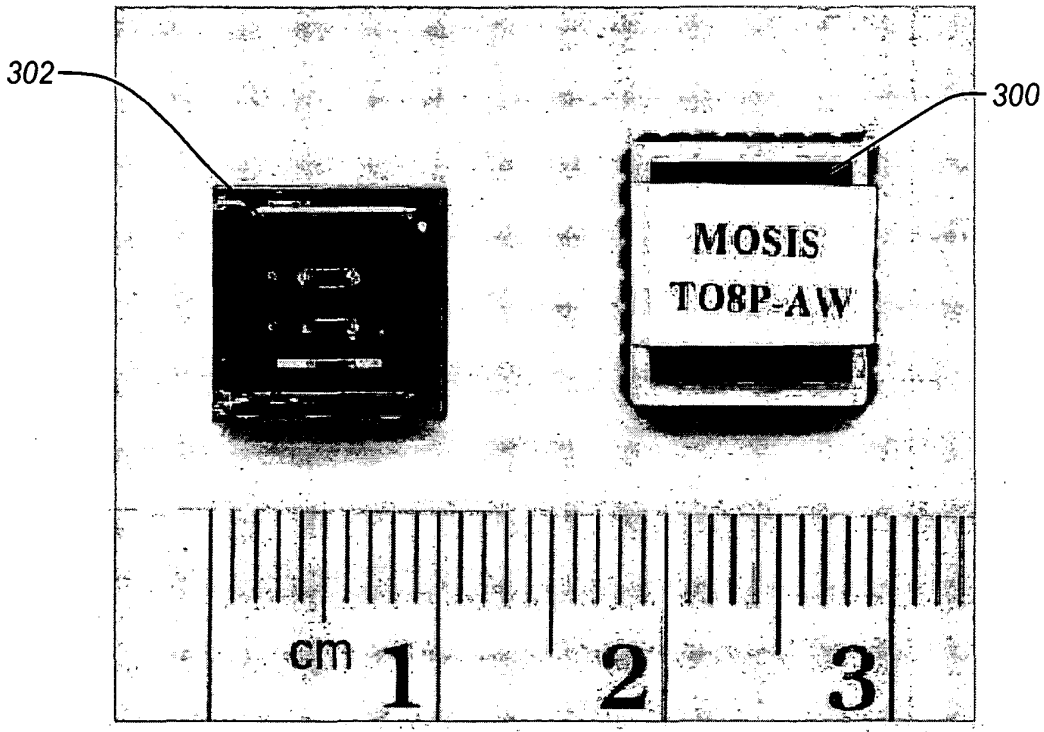

FIG. 3C

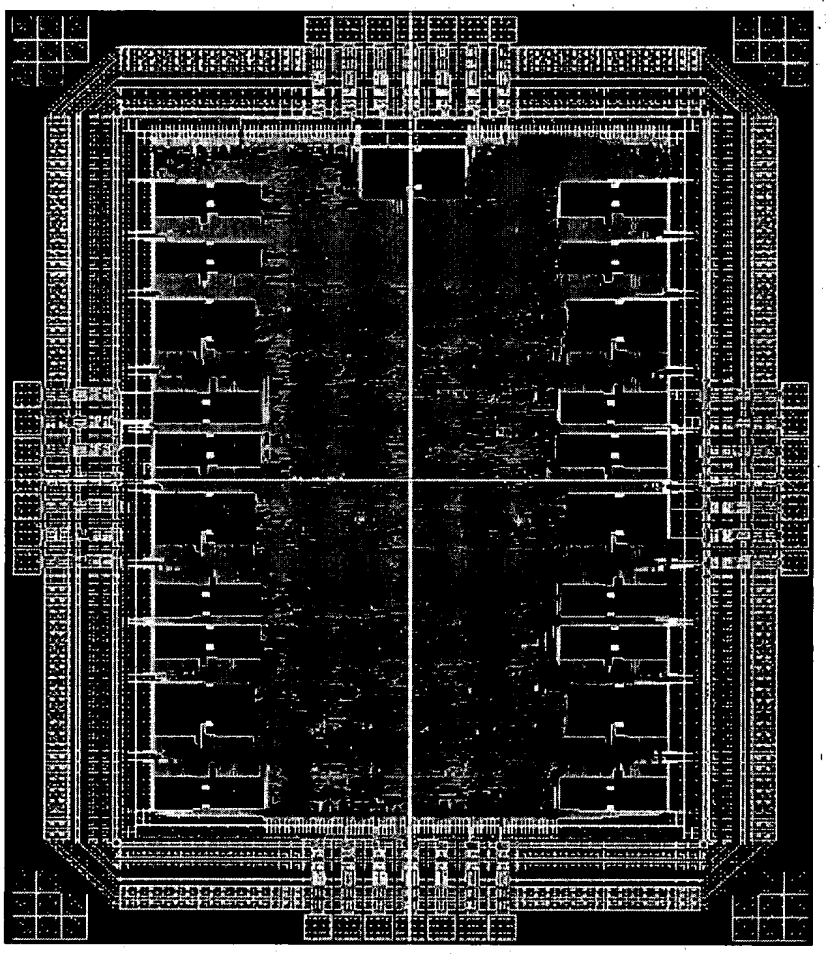

FIG. 3D

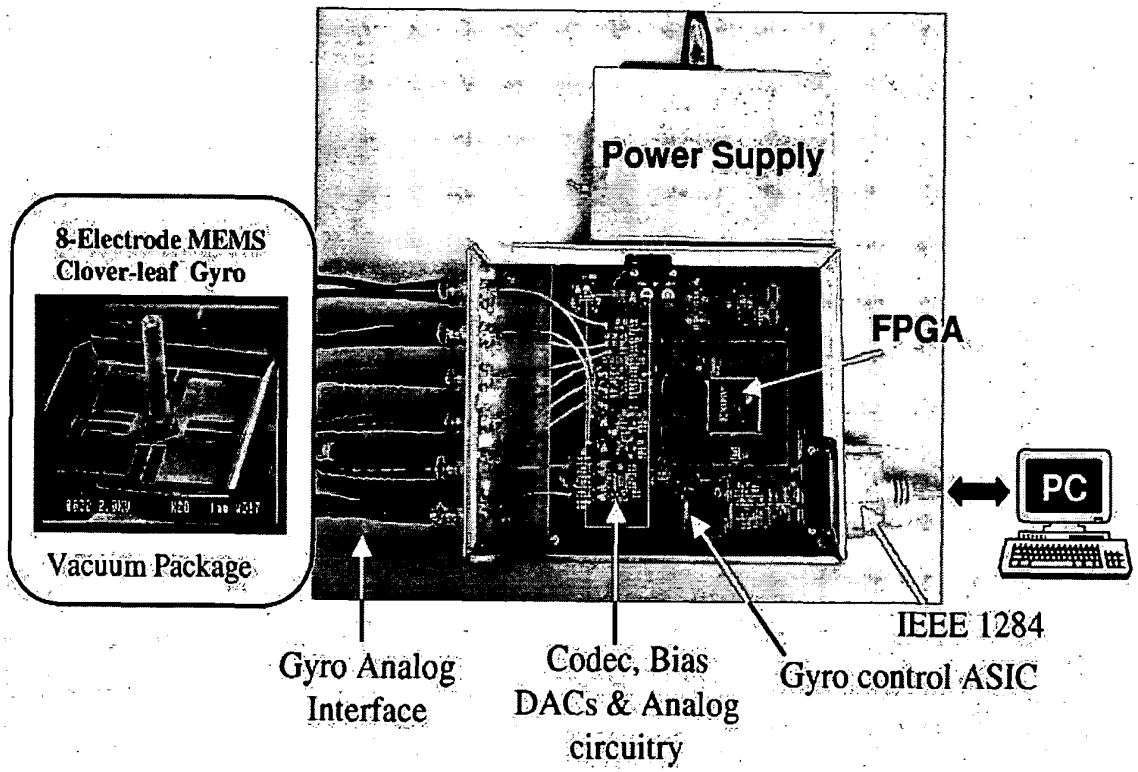
8-Electrode MEMS
Clover-leaf Gyro
Vacuum Package
Power Supply
FPGA
PC
IEEE 1284
Gyro Analog
Interface
Codec, Bias
DACs & Analog
circuitry
Gyro control ASIC

FIG. 4A

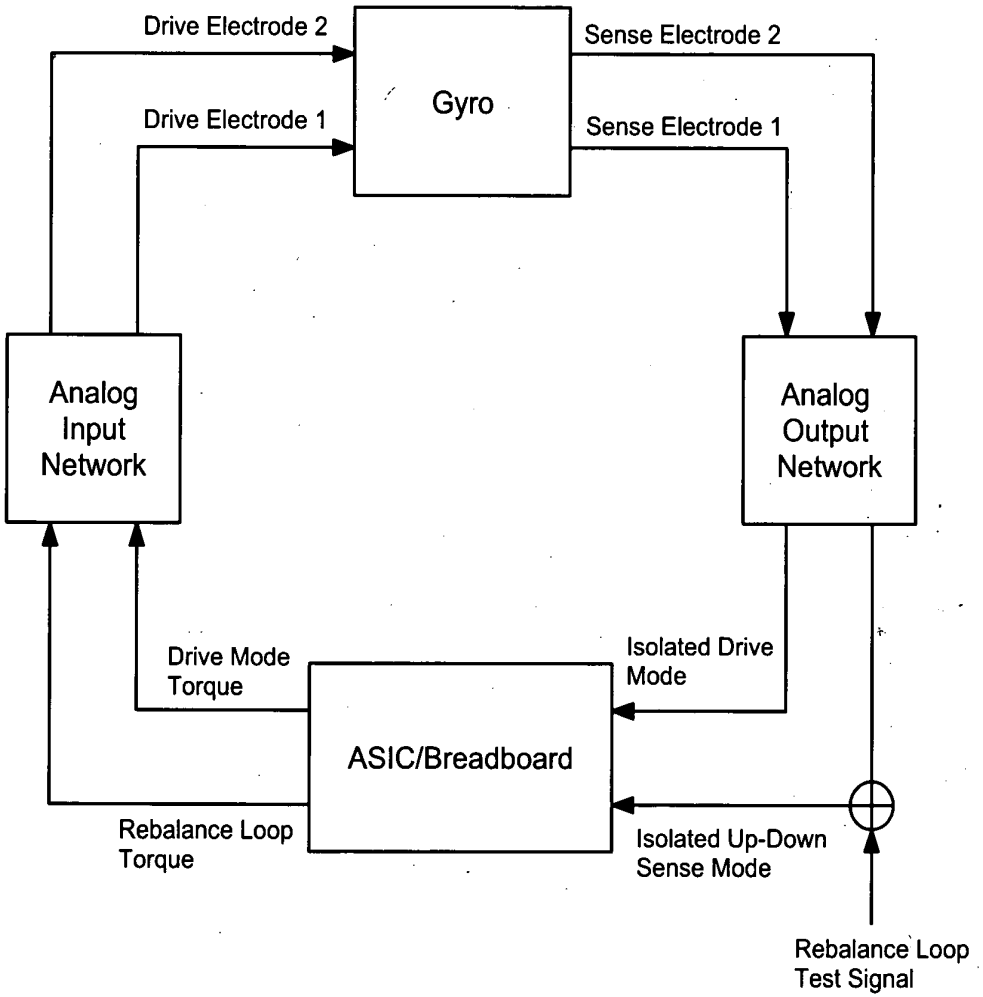
Drive Electrode 2
Drive Electrode 1
Gyro
Sense Electrode 2
Sense Electrode 1
Analog Input Network
Analog Output Network
Drive Mode Torque
Isolated Drive Mode
ASIC/Breadboard
Rebalance Loop Torque
Isolated Up-Down Sense Mode
Rebalance Loop Test Signal

FIG. 4B

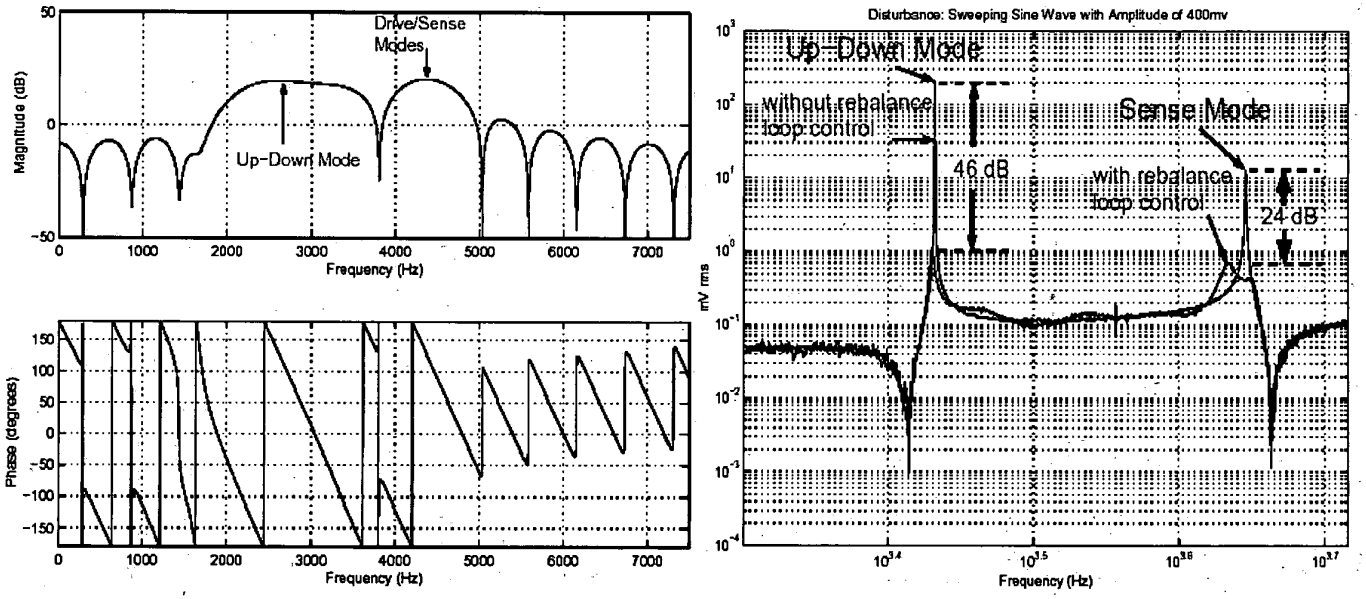
Drive/Sense
Modes
Up-Down Mode
Magnitude (dB)
Frequency (Hz)
Phase (degrees)
Frequency (Hz)
Disturbance: Sweeping Sine Wave with Amplitude of 400mv
Up-Down Mode
without rebalance
loop control
46 dB
Sense Mode
with rebalance
loop control
24 dB
mV rms
Frequency (Hz)

FIG. 4C

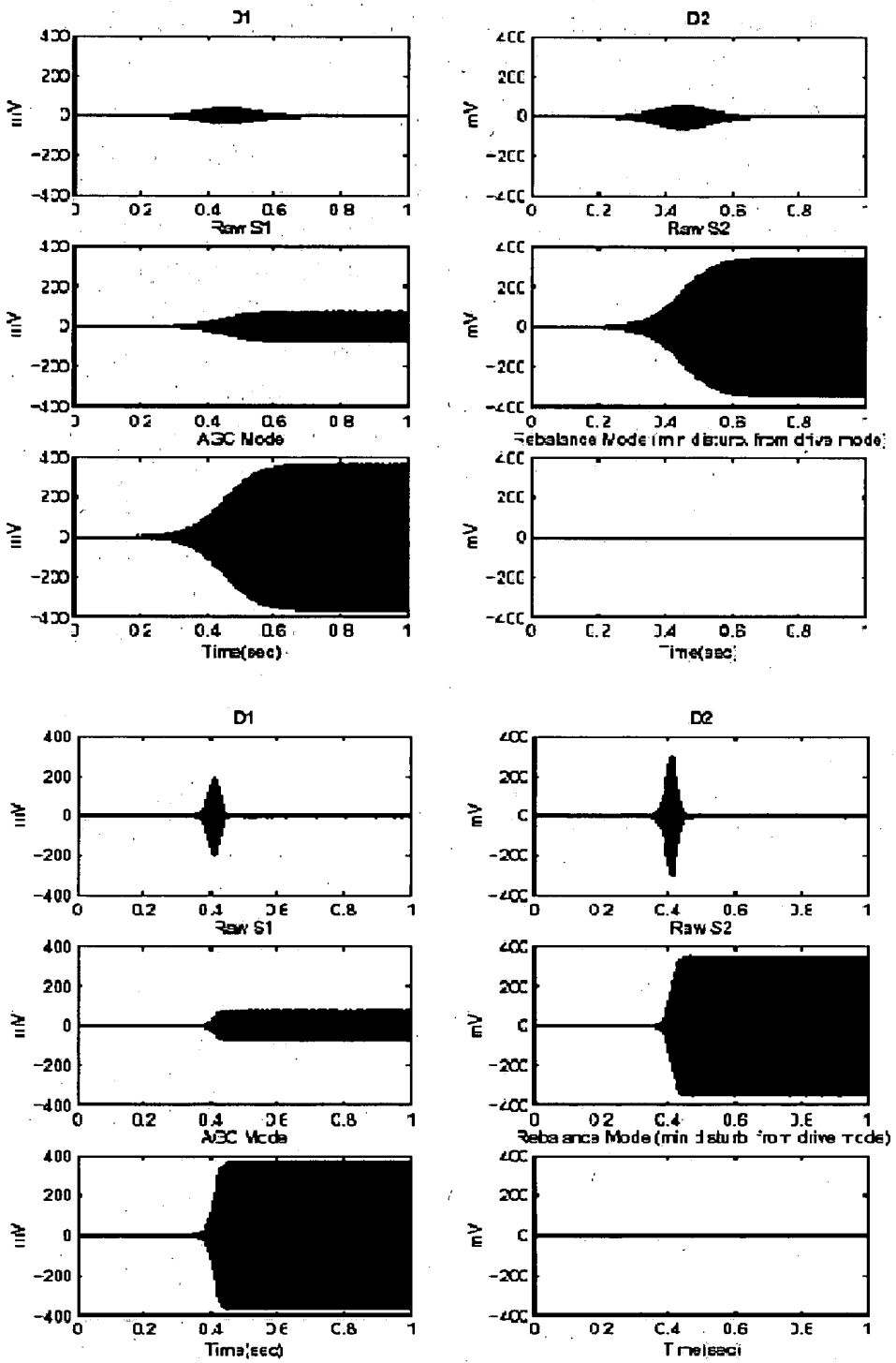
D1
D2
Raw S1
Raw S2
AGC Mode
Rebalance Mode (min disturb from drive mode)
Time(sec)
mV

FIG. 4D

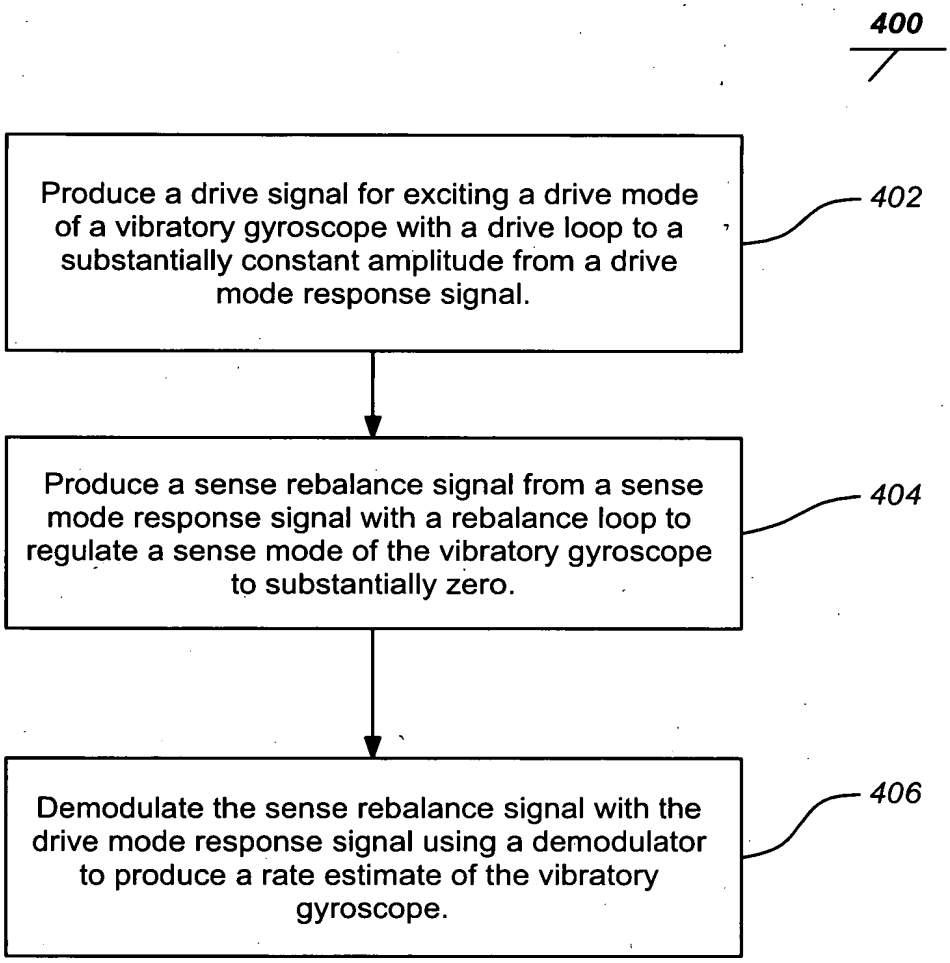
400
Produce a drive signal for exciting a drive mode of a vibratory gyroscope with a drive loop to a substantially constant amplitude from a drive mode response signal.
402
Produce a sense rebalance signal from a sense mode response signal with a rebalance loop to regulate a sense mode of the vibratory gyroscope to substantially zero.
404
Demodulate the sense rebalance signal with the drive mode response signal using a demodulator to produce a rate estimate of the vibratory gyroscope.
406

FIG. 4E